IN THE CLAIMS

1. (Currently amended) A memory device ~~(10)~~ comprising a memory ~~(24)~~ for storing memory data in memory sections allocated to address information, said memory ~~(24)~~ having a long read time compared to a write time, a read control unit ~~(16)~~ coupled with said memory ~~(24)~~ and adapted to read memory data in parallel from a plurality of sections or from all sections of the memory ~~(24)~~ that are defined by address information contained in an incoming write request, at least one first temporary memory ~~(20)~~ adapted to receive in parallel and store memory data, at least one second temporary memory ~~(14)~~ adapted to store at least a part of the data contained in the incoming write request directed to said memory, a comparator unit ~~(18)~~ coupled with said at least one first ~~(20)~~ and second ~~(24)~~ temporary memories and adapted to compare memory data stored in the first temporary memory ~~(20)~~ with data stored in the second temporary memory ~~(24)~~ and allocated to the same address information, and to provide an output indicative of the result of the respective comparison.

2. (Currently amended) The memory device of claim 1, wherein the read control unit ~~(16)~~ is adapted to sequentially perform a number of parallel-read operations from memory sections of the memory ~~(24)~~, such that all sections defined by address information contained in the incoming write request are covered by the number of read operations.

3. (Currently amended) The memory device of claim 1, wherein the read control unit ~~(16)~~ is adapted to start a parallel-read operation immediately after receiving address data contained in the write request.

4. (Currently amended) The memory device of claim 1, wherein the read control unit ~~(16)~~ is adapted to perform a parallel-read operation while the comparator unit ~~(18)~~ performs a comparison of write data stored in the at least one second temporary memory ~~(14)~~ with corresponding memory data in the at least one first temporary memory ~~(20)~~.

5. (Currently amended) The memory device of claim 4, wherein the at least one second temporary memory ~~(14)~~ has a storage capacity that is larger than that of the at least one first temporary memory ~~(20)~~ by a factor equal to the ratio of the read time and the write time.

6. (Currently amended) The memory device of claim 1, comprising a write control unit ~~(22)~~ that is coupled with the comparator unit ~~(18)~~ and the memory ~~(24)~~ and that is adapted to serially write only that write data to the memory for which the output of the comparator unit ~~(18)~~ indicates a difference to the corresponding memory data contained in the first temporary memory ~~(20)~~.

7. (Currently amended) The memory device of claim 6, wherein the write control unit ~~(22)~~ is adapted to perform a write operation as a direct-write operation or a toggle-write operation.

8. (Currently amended) The memory device of claim 6, wherein the read control unit ~~(16)~~ is adapted to perform a parallel-read operation while the write control ~~(22)~~ unit is

performing one or several write operations.

9. (Currently amended) The memory device of claim 1, wherein the memory ~~(24)~~ comprises 0T1MTJ memory cells.

10. (Currently amended) A method for comparing data stored in memory sections of a memory ~~(24)~~ with incoming data included in a write request, said memory ~~(24)~~ having a longer read time than write time, comprising the steps of a) receiving a write request comprising data and address information, said address information defining at least one memory section ~~(S10)~~, b) reading in parallel the data from a plurality of sections or from all sections of the memory that are defined by address information contained in the write request ~~(S12)~~, c) storing the memory data read in a first temporary memory ~~(S14)~~, d) storing at least a part of the data contained by the write request in a second temporary memory ~~(S16)~~, e) comparing the memory data contained in the first temporary memory with the corresponding data contained in the second temporary memory and allocated to the same address information ~~(S18)~~, f) providing an output indicative of the result of the comparison ~~(S20)~~.

11. (Currently amended) The method of claim 10, comprising a step of writing only that write data to the memory, for which the output indicates a difference from the corresponding memory data ~~(S22)~~.

12. (Currently amended) The method of claim 11, wherein the writing step ~~(S22)~~ is

performed as a direct-write or as a toggle-write operation.

13. (Currently amended) The method of claim 10, wherein steps b) ~~(S12)~~ and c) ~~(S14)~~ are performed in parallel with step d) ~~(S18)~~.

14. (Currently amended) The method of claim 10, wherein a number of parallel-read operations ~~(S12)~~ from memory sections of the memory is performed, such that all sections defined by address data contained in the incoming write request are covered by the number of read operations.

15. (Currently amended) The method of claim 10, wherein a parallel-read operation ~~(S12)~~ is performed immediately after receiving address data ~~(S10)~~ contained in the write request.

16. (Currently amended) The method of claim 10, wherein write data is written ~~(S22)~~ serially to the memory.

17. (Currently amended) The method of claim 10, wherein a parallel-read operation ~~(S12)~~ is performed while one or several write operations ~~(S22)~~ are performed.

18. (Currently amended) The method of claim 10, performed in an MRAM memory with 0T1MTJ memory cells ~~(24)~~.